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ATTENTION:	*Examiner:* _____ *Art Unit:* _____	

FROM:	TELEPHONE NO.:
David Cordeiro, Reg. No. 48,134	(408) 474 - 9057

RE:		
	Serial No.:	10/502,407
	Attorney Docket No.:	DE02 0024

TRANSMISSION INCLUDES: 32 Pages (including cover sheet)

Petition to Withdraw Abandonment – 2 pages

Notice of Abandonment – 1 page

Filing Package with Transmittal Letter – 28

CERTIFICATE OF TRANSMISSION UNDER 37 CFR 1.8

I hereby certify that this correspondence is being facsimile transmitted to the Patent and Trademark Office at the number listed above

on 3/19/07 2007 by _____
Vilimaina Naga

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1109 McKay Drive
San Jose, CA 95131
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First-Named Inventor: Robert Tolkiehn	Docket No.: DE02 0024 US
Application No.: 10/502,407 Conf.: 3922	Art Unit:
Date Filed: 07/22/2004	Examiner:

Title: CIRCUIT CONFIGURATION AND METHOD OF GENERATING THE DRIVE SIGNAL OF THE DEFLECTION TRANSISTOR OF A CATHODE RAY TUBE

PETITION TO WITHDRAW ABANDONMENT UNDER MPEP SECTION 711.03(c)

Sir:

Applicant(s) hereby petition to withdraw the holding of abandonment as evidenced by the Notice of Abandonment dated 05/20/2005 (copy attached).

The holding of abandonment is in error for the following reasons.

In response to the Notification of Abandonment, the full U.S. Basic National Fee with authorization to charge to Deposit Account 14-1270, and a Certificate of Mailing, was transmitted by Applicant(s) Attorney on July 22, 2004 (a copy is enclosed).

The holding of abandonment was in error, and Applicant(s) hereby petition for its withdrawal.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

The Commissioner is hereby requested and authorized pursuant to 37 CFR §1.136(a)(3), to treat any concurrent or future reply in this application requiring a petition for extension of time for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. Please charge any additional fees which may now or in the future be required in this application, including extension of time fees, but excluding the issue fee unless explicitly requested to do so, and credit any overpayment, to Deposit Account No. 50-4019

Date: 3/19/07

Respectfully submitted,

By _____

David Cordeiro, Reg. No. 48,134
NXP B.V.
1109 McKay Drive, M/S-41SJ
San Jose, California 95131
(408) 474-9057

Enclosures:
- ☒ Copy of Abandonment
- ☒ Copy of Transmittal Letter authorizing to Charge Deposit Account
- ☒ Authorization to charge fees to deposit account 50-4019

UNITED STATES PATENT AND TRADEMARK OFFICE

S1M0

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U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
10/502,407	Robert Tolkiehn	DE02 0024 US

INTERNATIONAL APPLICATION NO.	
PCT/IB02/00183	
I.A. FILING DATE	PRIORITY DATE
01/22/2003	02/01/2001

Philips Electronics North America Corporation
Intellectual Property & Standard
1109 McKay Drive, M/S41-SJ
San Jose, CA 95131

CONFIRMATION NO. 3922

371
ABANDONMENT/TERMINATION LETTER

OC000000016026059

Date Mailed: 05/20/2005

NOTIFICATION OF ABANDONMENT

The United States Patent and Trademark Office in its capacity as a Designated / Elected Office (37 CFR 1.495) has made the following determination:

- Applicant has failed to provide the full U.S. Basic National Fee by 30 months (37 CFR 1.495(b)(2)).

Therefore, the above identified application failed to meet the requirements of 35 U.S.C. 371 and 37 CFR 1.495,and is ABANDONED AS TO THE UNITED STATES OF AMERICA.

CHARITTA A BURT

Telephone: (703) 308-9140 EXT 207

PART 1 - ATTORNEY/APPLICANT COPY

FORM PCT/DO/EO/909 (371 Abandonment Notice)

SL MAY 2005

SJC MAY 27 2005

Pet. to Revive 7/20

Express Mail:	EV508238700US	*Docket No.:*	DE02 0024 US
Int'l. Filing Date:	22 January 2003	*Date Mailed:*	7/22/04
First Inventor:	TOLKIEHN, Robert	*Attorney:*	SIMO / dlm

Title:

"Circuit configuration and method of generating the drive signal of the deflection transistor of a cathode ray tube"

Items listed have been received in the USPTO on the date indicated by the stamp below.

- ☒ Transmittal Letter ☒ Cert. of Mailing
- ☒ Fees paid by deposit account
- ☒ PCT Application - 11 pages
  - ☒ Includes specification, 17 claims & abstract
- ☒ 3 sheets of Drawings ☐ Letter to Off. Draftsman
- ☒ Preliminary Amendment - 5 pages
- ☐ Assignment with Recordation Form Cover Sheet – Fees paid
- ☐ Declaration & POA – 1 page
- ☒ IDS with Form PTO-1449 ☒ copy of 3 cited refs.
- ☒ Power of Attorney to Prosecute Application Before the USPTO
- ☒ Statement Under 37 CFR 3.73(b)

JUL 28 2004

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Label 11-F June 2002

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DANIEL L. MICHALIK
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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		ATTORNEY'S DOCKET NO. DE02 0024 US U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
INTERNATIONAL APPLICATION NO. PCT/IB02/00183	INTERNATIONAL FILING DATE 22 January 2003	PRIORITY DATE CLAIMED 26 January 2002

TITLE OF INVENTION
Circuit configuration and method of generating the drive signal of the deflection transistor of a cathode ray tube

APPLICANT(S) FOR DO/EO/US
Koninklijke Philips Electronics N.V.

Applicant(s) herewith submit to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2))
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendment to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet is compliance with 37 C.F.R. 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND OR SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information:
    ☒ Power of Attorney to Prosecute Application Before the USPTO [PTO/SB/90]
    ☒ Statement under 37 CFR 3.73(b) [PTO/SB/96]
    ☒ Authorization Pursuant to 37 CFR § 1.136(a)(3) and to Charge Deposit Account 14-1270.
    3 Sheet(s) of Drawings

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to "Mail Stop PCT, Commissioner for Patents, PO Box 1450, Arlington, VA 22313," on the date indicated below.

(Date) 7/22/04 (Signature) _____
Daniel L. Michalik

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)	INTERNATIONAL FILING NO.	ATTORNEY'S DOCKET NUMBER
	PCT/IB02/00183	DE02 0024 US

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 C.F.R. 1.492(A)(1)-(5)):		
Search Report has been prepared by the EPO or JPO $860.00		
International preliminary-examination fee paid to USPTO (37 CFR 1.482)..... $690.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)..... $750.00		
Neither international preliminary examination fee (37 C.F.R.1.482) nor international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO $970.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4)..... $96.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =..... 970.00		
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).	$0.00	

CLAIMS	NUMBER FILED	# EXTRA	RATE		
Total Claims	17 - 20 =	0	x $ 18.00	$0.00	
Independent claims	1 - 3 =	0	x $ 84.00	$0.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)		0	+ $280.00	$0.00	
			TOTAL OF ABOVE CALCULATIONS =	$970.00	
Reductions by 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 C.F.R. 1.9, 1.27, 1.28)				$0.00	
			SUBTOTAL =	$970.00	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(f)). +				$0.00	
			TOTAL NATIONAL FEE =	$970.00	
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28,3.31). $40.00 per property +				$40.00	
			TOTAL FEES ENCLOSED =	$1010.00	
			Amount to be Refunded	$	
			Charged	$	

☒ Please charge my **Deposit Account No. 14-1270 (Customer No. 24737)** in the amount of **$1010.00** to cover the above fees. A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any additional fee, with the exception of the Base Issue Fee, which may be required, or credit any overpayment to **Deposit Account No. 14-1270**. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
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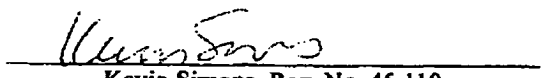
San Jose, California 95131



Kevin Simons, Reg. No. 45,110
Tel.: (408) 474-9075

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	Unassigned	Confirmation No.	Unassigned
Applicant	:	TOLKIEHN, Robert		
Filed	:	Concurrently		
TC/A.U.	:	Unassigned		
Examiner	:	Unassigned		
Docket No.	:	**DE02 0024 US**		
Customer No.	:	24738		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination please amend the above-identified application as follows:

Amendments to the Specification there are no amendments in this paper.

Amendments to the Claims begin on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

8. (CURRENTLY AMENDED) A method of operating a circuit configuration, in particular a circuit configuration as claimed in claim 1 ~~any one of claims 1 to 3~~, characterized in that the target phase ~~(ZP3)~~ of the second phase-locked loop ~~(PLL2)~~ is constant.

9. (CURRENTLY AMENDED) A method as claimed in claim 8, characterized in that the target phase ~~(ZP3)~~ of the second phase-locked loop ~~(PLL2)~~ is 10%.

10. (CURRENTLY AMENDED) A method of operating a circuit configuration, in particular a circuit configuration as claimed in ~~any one of claims 1 to 3,~~ claim 1 characterized in that the dynamic component of the target phase ~~(ZP3)~~ of the second phase-locked loop ~~(PLL2)~~ is less than 20% of the entire horizontal modulation. ~~(hmod).~~

11. (CURRENTLY AMENDED) A method of operating a circuit configuration, in particular a circuit configuration as claimed in ~~any one of claims 1 to 3,~~ claim 1 characterized in that the dynamic component of the target phase (ZP3) of the second phase-locked loop (PLL2) is approximately 7% of the entire horizontal modulation (hmod).

12. (CURRENTLY AMENDED) A method of operating a circuit configuration, in particular a circuit configuration as claimed in ~~any one of claims 1 to 3,~~ claim 1 characterized in that the adjustment of the horizontal modulation ~~(hmod)~~ takes place in two parts ~~(hmod1 and hmod2),~~ wherein the first part (hmod1) is realized in the first delay block ~~(DB1),~~ and the second part ~~(hmod2)~~ is realized in the second phase-locked loop. ~~(PLL2).~~

13. (CURRENTLY AMENDED) A method as claimed in claim 12, characterized in that the first part ~~(hmod1)~~ realizes the larger component of the adjustment of the horizontal modulation ~~(hmod),~~ and the second part ~~(hmod2)~~ realizes the smaller component.

Amendments to the Claims

1. (CURRENTLY AMENDED) A circuit configuration for generating the drive signal of the deflection transistor of a cathode ray tube comprising a two-PLL system, characterized in that a delay block ~~(DB1)~~ is connected between the first and the second phase-locked loop. ~~(PLL1, PLL2).~~

2. (CURRENTLY AMENDED) A circuit configuration as claimed in claim 1, characterized in that the output ~~(HREF)~~ of the first phase-locked loop ~~(PLL1)~~ is connected to the input of the delay block ~~(DB1).~~

3. (CURRENTLY AMENDED) A circuit configuration as claimed in claim 1 ~~or 2~~, characterized in that the output of the first delay block ~~(DB1)~~ is connected to an input of the second phase-locked loop. ~~(PLL2).~~

4. (CURRENTLY AMENDED) A method of operating a circuit configuration, in particular a circuit configuration as claimed in claims 1 ~~to 3~~, characterized in that the horizontal modulation ~~(hmod)~~ is a control value for the delay block. ~~(DB1).~~

5. (CURRENTLY AMENDED) A method as claimed in claim 4, characterized in that, together, the constant component ~~(const1)~~ of the target phase ~~(ZP1)~~ of the first phase-locked loop ~~(PLL1)~~ and the constant component ~~(const2)~~ of the first delay block ~~(DB1)~~ are greater than 100%.

6. (CURRENTLY AMENDED) A method as claimed in claim ~~4 or 5~~, characterized in that the constant component ~~(const1)~~ of the first phase-locked loop PLL1 is 30%.

7. (CURRENTLY AMENDED) A method as claimed in claim 4 ~~any one of claims 1 to 6~~, characterized in that the constant component ~~(const2)~~ of the first delay block ~~(DB1)~~ is 80%.

14. (CURRENTLY AMENDED) A method as claimed in claim 13, characterized in that the first part ~~(hmod1)~~ is 14% and the second part ~~(hmod2)~~ is 1%.

15. (CURRENTLY AMENDED) A method as claimed in ~~any one of claims 4 to 14,~~ claim 4 characterized in that the horizontal modulation ~~(hmod)~~ is 15%.

16. (CURRENTLY AMENDED) A method as claimed in ~~any one of claims 12 to 15,~~ claim 12 characterized in that the target phase ~~(ZP2)~~ for the first delay block ~~(DB1)~~ lies in a range from 66% to 94%, and the target phase ~~(ZP3)~~ for the second phase-locked loop ~~(PLL2)~~ lies in a range from 9% to 11%.

17. (CURRENTLY AMENDED) A method as claimed in ~~any one of claims 4 to 16,~~ claim 4 characterized in that the circuit configuration is implemented digitally.

REMARKS/ARGUMENTS

The foregoing amendment(s) to claim(s) was/were made solely to avoid filing the claim in the multiple dependent form so as to avoid the additional filing fee.

The claim(s) was/were not amended in order to address issues of patentability and Applicant respectfully reserves all rights she may have under the Doctrine of Equivalents. Applicant furthermore reserves her right to reintroduce subject matter deleted herein at a later time during the prosecution of this application or continuing applications.

Please charge any fees other than the issue fee and credit any overpayments to Deposit Account 14-1270.

Respectfully submitted,

Date: 7/20/2004

By _____
Kevin Simons, Reg. No. 45,110
(408) 474-9075

Correspondence Address:

Intellectual Property & Standards
Philips Electronics North America Corporation
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131 USA

24738
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Circuit configuration and method of generating the drive signal of the deflection transistor of a cathode ray tube

The invention relates to a circuit configuration for generating the drive signal (HDRV = horizontal drive) for the deflection transistor that drives the oscillating circuit for the horizontal deflection of a cathode ray tube (CRT = cathode ray tube). The horizontal synchronization signal (HSYNC) and the horizontal flyback (HFB) are used as the input signals for the circuit configuration. The horizontal flyback is hereby proportional to the oscillating circuit voltage. Circuit configurations of this kind may be implemented as analog or digital.

The invention relates, in particular, to a circuit configuration that uses two phase-lock loops (PLLs). The first of these phase-lock loops hereby generates an internal, low-interference reference. The second of these phase-lock loops controls the phase angle of the loop "internal reference – horizontal drive (HDRV) – deflection transistor – oscillating circuit and horizontal flyback (HFB)". By contrast with the first control loop, this second control loop follows the dynamic, horizontal modulation, which is visible on the monitor by means of parallelogram setting, for instance. The second control loop has a very much smaller time constant T_{loop2}. It is known from the described circuit configuration for the generation of the drive signal of a deflection transistor and from other realizations that, in the ideal case, firstly, the horizontal position (hpos = horizontal position) and, secondly, the horizontal modulation (hmod = horizontal modulation) should each have an adjustment range of up to ±15%. A further, third requirement is that the horizontal duty time of the deflection transistor should be up to 60% and its storage time up to 30%. For example, approximately 2 msec storage time corresponds to 30% of the period at 140 kHz sweep frequency. In the known systems, all three of these requirements cannot be fulfilled. The overall coherence of the system means that an improvement of the value for one of the requirements leads to a deterioration of one of the other values.

The conventional circuit configuration for generating the drive signal for the deflection transistor has proved its worth, but the broad adjustment ranges required for the

horizontal position and the horizontal modulation in deflection transistors having long duty times and storage times cannot be achieved without increasing the back coupling of the second phase-lock loop by one period. This delaying of the reaction time would lead to a deterioration of the control response of the second phase-lock loop, and is generally not acceptable.

It is therefore the object of the invention to specify a circuit configuration which achieves the broad adjustment ranges required for the horizontal position and the horizontal modulation, even for a deflection transistor with a long duty time and storage time, without increasing the delay of the back coupling of the second control loop.

This object is achieved in accordance with the invention in that a first delay block is connected between the output of the first phase-lock loop and the input of the second phase-lock loop. The input signal of the delay block is the horizontal reference, and the output signal is a delayed, second horizontal reference, which is, in turn, an input signal of the second phase-lock loop. Together, the constant component of the first phase-lock loop and the constant component of the first delay block amount to more than 100%. The circuit configuration in accordance with the invention gives rise to a change in the phase measurement of the second phase-lock loop: the phase of the horizontal flyback is now measured against the delayed, second horizontal reference rather than against the single horizontal reference, as with the conventional circuit configuration.

The principle and advantage of the invention is that, for all horizontal positions (hpos) and horizontal modulations (hmod) together, i.e. for the range for hpos+hmod of −30% to +30%, the delayed, second horizontal reference lies between the occurrence of the horizontal flyback (HFB) and the start of the horizontal drive signal (HDRV) for the deflection transistor. This means that, following expiry of the horizontal flyback, the phase measurement can immediately proceed to the generation of the next horizontal drive signal (HDRV), and therefore a minimal delaying of the control loop (minimal loop latency) is achieved. With a required storage time of 60% and a duty time of 30%, it is thereby possible always to undertake phase measurement in the 10% slot remaining. The phase measurement thereby does not restrict the adjustment range of the horizontal modulation (hmod).

One further advantage of the circuit configuration in accordance with the invention is that the phase angle of the signals is always such that the phase detectors in the

two phase-lock loops initially measure the time of occurrence of the horizontal synchronization signal (HSYNC) and the horizontal flyback (HFB), then measure the time of occurrence of the first horizontal reference and the second horizontal reference, and finally produce the difference between these. The phase detectors are simplified as a result, especially in the case of digital implementations.

The invention will be further described with reference to examples of embodiments shown in the drawings, to which, however, the invention is not restricted.

Fig. 1 shows, in sub-figures a) and b), a block circuit diagram 1 of the circuit configuration in accordance with the invention with different control values.

Fig. 2 shows the signal waveform of the horizontal synchronization signal over time.

Fig. 3 shows the signal waveform of the horizontal reference over time.

Fig. 4 shows the signal waveform of the second horizontal reference over time.

Fig. 5 shows the signal waveform of the drive signal over time.

Fig. 6 shows the signal waveform of the horizontal flyback over time.

The signal waveforms in Figs. 2 to 6 represent the steady state.

The block diagram 1 of a two-PLL system shown in Fig. 1a) comprises a first phase-lock loop PLL1, a first delay block DB1, a second phase-lock loop PLL2, a second delay block DB2, and an RS flip-flop FF. An output of the first phase-lock loop PLL1 is connected to an input of the first delay block DB1. An output of the first delay block DB1 is connected to an input 2 of the second phase-lock loop PLL2. An output of the second phase-lock loop PLL2 is branched and led to an input S of an RS flip-flop FF and to an input of a second delay block DB2. An output of the second delay block DB2 is connected to an input R of the RS flip-flop FF. The two-PLL system described below is used, in particular, for the horizontal deflection of a cathode ray tube. Interface signals to the remaining system are the horizontal synchronization HSYNC, the drive signal HDRV for the deflection transistor and the horizontal flyback HFB. The drive signal HDRV, which is generated by the circuit configuration in accordance with the invention, switches the deflection transistor on and off.

The horizontal flyback HFB represents the position of the electronic ray on the monitor. Control values for the system shown are:

- for the first phase-lock loop PLL1:

as target phase ZP1: the horizontal position hpos, plus a constant component const1, which is generated in the first phase-lock loop and, in this embodiment example, is 30%, and

the quasi-static horizontal position, which is preset by the overall system, and is hpos = ±15%, so that ZP1 = 15% to 45%.

- for the delay block DB1:

as target phase ZP2: the dynamic horizontal modulation hmod, plus a constant component const2, which is generated in the first delay block and, in this embodiment example, is 80%, and

the horizontal modulation hmod, which is preset by the overall system, and is hmod = ±15%, so that ZP2 = 65% to 95%.

- for the second phase-lock loop PLL2:

as target phase ZP3: a constant component const3, which is generated in the second phase-lock loop and, in this embodiment example, is 10%, so that ZP3 also = 10%.

- for the second delay block DB2:

as target phase ZP4: the quasi-static horizontal duty time hduty, which is preset by the overall system, so that ZP4 = hduty = 40% to 60%.

The block diagram 1 shown in Fig. 1b) comprises the same elements as shown in Fig. 1a). The difference consists in the control values for delay block DB1 and the second phase-lock loop PLL2. In this embodiment example, control values for these are as follows:

- for delay block DB1:

as target phase ZP2: the first dynamic horizontal modulation hmod1 plus a constant component const2, which is generated in the first delay block and, in this embodiment example, is 80%, and

the first horizontal modulation hmod1, which is preset by the overall system and is hmod1 = ±14%, so that ZP2 = 66% to 94%.

- for the second phase-lock loop PLL2:

as target phase ZP3: the second horizontal modulation hmod2 plus a constant component const3, which is generated in the second phase-lock loop and, in this embodiment example, is 10%, and

the second horizontal modulation, which is preset by the overall system, and is hmod2 = ±1%, so that ZP3 = 9% to 11%.

In this embodiment example in accordance with Fig. 1b), adjustment of the horizontal modulation hmod takes place in two parts, hmod1 and hmod2; wherein hmod = hmod1+hmod2. It is preferred that the larger part hmod1 of, for example, +/- 14% is realized in the first delay block DB1, and the smaller part hmod2 of, for example, +/- 1% is realized in the second phase-lock loop PLL2. Owing to the division of the horizontal modulation, values that are especially suited to a digital implementation arise.

Fig. 2 shows the signal waveform of the horizontal synchronization signal HSYNC. A period interval identified as 100% starts and ends with the leading edge of a square-wave signal. The pulse duration is generally less than 25% and the leading edge or the center of the horizontal synchronization signal HSYNC is generally used as the reference point.

Fig. 3 shows the signal waveform of the internal, low-interference, horizontal reference HREF (= horizontal reference). The influence of target phase ZP1 of 15% to 45% on the output signal HREF of the first phase-lock loop PLL1 is shown with a dotted line. The square-wave pulse shown with a solid line illustrates the influence of constant component const1 = 30% in the case of hpos = 0%. The square-wave pulses at approximately 15% and approximately 45% show that the boundaries of the adjustment range of horizontal position hpos, which should fulfill the requirements of ±15%, have been reached, i.e. they are shifted 30% in order that they are only positive.

Fig. 4 shows the signal waveform of the delayed, second horizontal reference HREF2. In the example shown, the component, measured from the input signal HREF of delay block DB1 onwards, is const2 = 80%. This means that, in the case where hpos = 0% and hmod = 0%, viewed over a period interval of 100%, the leading edge of the square-wave signal of the second horizontal reference HREF2 appears at 10% of a period interval after the leading edge of the horizontal synchronization signal. This derives from formula 1:

$$30\%\ (HREF) + 80\%\ (HREF2) - 100\%\ (HSYNC) = 10\%\ (HFB) \qquad (1)$$

The maximum influence of the reference input variable hpos = ±15% is illustrated by the square-wave pulse shown with a dotted line to the right and left of the square-wave pulse shown with a solid line for hpos = 0%. The maximum effect of reference input variable hmod = ±15% is shown by the square-wave pulse shown with a dotted line to the right and left externally. The requirement for hmod can therefore be fulfilled in addition to the requirements for hpos, both requirements are ±15%.

Fig. 5 shows the signal waveform of the generated drive signal HDRV for the deflection transistor. The solid line shows the maximum pulse duration of 60%. The segments shown with dotted lines represent drive signal HDRV at a maximum pulse duration of 60% for the cases (hpos+hmod) = -30%, -15%, +15% and +30%.

Fig. 6 shows the signal waveform of the horizontal flyback HFB. In the example shown with a solid line, the horizontal flyback is in phase with the horizontal synchronization signal. Horizontal flyback HFB always appears with a delay constituting the storage time after switch-off of the deflection transistor (trailing edge of HDRV). Accordingly, the phase angle of horizontal flyback HFB varies in accordance with that of drive signal HDRV.

In a preferred embodiment of the invention, target phase ZP3 of the second phase-lock loop PLL2 is constant, e.g. 10%, and the horizontal modulation hmod is realized exclusively in target phase ZP2 of delay block DB1.

In a variant for operating the circuit configuration in accordance with the invention, target phase ZP2 for the first delay block DB1 lies in a range comprising the first part hmod1 and a constant component const2, so that ZP2 = hmod1 +80%. For hmod1, ±14% is preferably selected, thereby giving rise to a range from 66% to 94% for target phase ZP2. In addition, with this variant, target phase ZP3 for the second phase-lock loop PLL2 lies in a range formed from the second part and a constant component const3, so that ZP3 = hmod2 + 10%. For hmod2, ±1% is preferably selected, thereby giving rise to a range from 9% to 11% for target phase ZP3. This variant is particularly suited to digital implementation.

The circuit configuration in accordance with the invention generates a second horizontal reference signal HREF2, which, viewed over time, lies between the square-wave signal of the horizontal flyback and the square-wave signal of the drive signal for the deflection transistor for all horizontal positions hpos and horizontal modulations hmod together, i.e. for the range from hpos+hmod = -30% to hpos+hmod = +30%. For long storage times, e.g. $T_{STORAGE}$ = 30%, of the deflection transistor, and for long duty times, e.g. hduty = 60%, a time of 10% remains for the phase measurement and back coupling of the second phase-lock loop PLL2.

In summary, for the circuit configuration in accordance with the invention with a delay block DB1, a larger range for the horizontal modulation, more duty time and/or more storage time are acceptable for the positioning of the second horizontal reference signal HREF2 between the horizontal flyback HFB and the generated drive signal HDRV as

compared with the prior art, without extending the delay of the back coupling of the phase-lock loop to more than one period interval.

CLAIMS:

1. A circuit configuration for generating the drive signal of the deflection transistor of a cathode ray tube comprising a two-PLL system, characterized in that a delay block (DB1) is connected between the first and the second phase-locked loop (PLL1, PLL2).

2. A circuit configuration as claimed in claim 1, characterized in that the output (HREF) of the first phase-locked loop (PLL1) is connected to the input of the delay block (DB1).

3. A circuit configuration as claimed in claim 1 or 2, characterized in that the output of the first delay block (DB1) is connected to an input of the second phase-locked loop (PLL2).

4. A method of operating a circuit configuration, in particular a circuit configuration as claimed in claims 1 to 3, characterized in that the horizontal modulation (hmod) is a control value for the delay block (DB1).

5. A method as claimed in claim 4, characterized in that, together, the constant component (const1) of the target phase (ZP1) of the first phase-locked loop (PLL1) and the constant component (const2) of the first delay block (DB1) are greater than 100%.

6. A method as claimed in claim 4 or 5, characterized in that the constant component (const1) of the first phase-locked loop PLL1 is 30%.

7. A method as claimed in any one of claims 4 to 6, characterized in that the constant component (const2) of the first delay block (DB1) is 80%.

8. A method of operating a circuit configuration, in particular a circuit configuration as claimed in any one of claims 1 to 3, characterized in that the target phase (ZP3) of the second phase-locked loop (PLL2) is constant.

9. A method as claimed in claim 8, characterized in that the target phase (ZP3) of the second phase-locked loop (PLL2) is 10%.

10. A method of operating a circuit configuration, in particular a circuit configuration as claimed in any one of claims 1 to 3, characterized in that the dynamic component of the target phase (ZP3) of the second phase-locked loop (PLL2) is less than 20% of the entire horizontal modulation (hmod).

11. A method of operating a circuit configuration, in particular a circuit configuration as claimed in any one of claims 1 to 3, characterized in that the dynamic component of the target phase (ZP3) of the second phase-locked loop (PLL2) is approximately 7% of the entire horizontal modulation (hmod).

12. A method of operating a circuit configuration, in particular a circuit configuration as claimed in any one of claims 1 to 3, characterized in that the adjustment of the horizontal modulation (hmod) takes place in two parts (hmod1 and hmod2), wherein the first part (hmod1) is realized in the first delay block (DB1), and the second part (hmod2) is realized in the second phase-locked loop (PLL2).

13. A method as claimed in claim 12, characterized in that the first part (hmod1) realizes the larger component of the adjustment of the horizontal modulation (hmod), and the second part (hmod2) realizes the smaller component.

14. A method as claimed in claim 13, characterized in that the first part (hmod1) is 14% and the second part (hmod2) is 1%.

15. A method as claimed in any one of claims 4 to 14, characterized in that the horizontal modulation (hmod) is 15%.

16. A method as claimed in any one of claims 12 to 15, characterized in that the target phase (ZP2) for the first delay block (DB1) lies in a range from 66% to 94%, and the target phase (ZP3) for the second phase-locked loop (PLL2) lies in a range from 9% to 11%.

17. A method as claimed in any one of claims 4 to 16, characterized in that the circuit configuration is implemented digitally.

ABSTRACT:

Circuit configuration for generating the drive signal (HDRV) for the deflection transistor that drives the oscillating circuit for the horizontal deflection of a cathode ray tube (CRT). The circuit configuration in accordance with the invention generates a second, horizontal reference signal (HREF2), which, viewed over time, lies between the signal for the horizontal flyback (HFB) and the square-wave signal of the drive signal (HDRV) for the deflection transistor, for all possible horizontal positions (hpos) and horizontal modulations (hmod). Connected between the output of the first phase-lock loop (PLL1) and the input of the second phase-lock loop (PLL2) is a delay block (DB1). In accordance with the invention, the phase measurement of the horizontal flyback (HFB) in relation to the second horizontal reference signal (HREF2) always takes place in the time constituting 10% of a period. For the positioning of the second horizontal reference signal (HREF2), the first delay block (DB1) is, in accordance with the invention, added to the conventional circuit configuration.

Fig. 1a

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Assignee Name and Address:

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SIGNATURE of Assignee of Record
The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Name	Matthieu van Kaam		
Signature		Date	April 19, 2004
Title	Authorized Representative	Telephone	(914) 333-9600

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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Koninklijke Philips Electronics N.V.

Application No./Patent No.: Concurrently Filed/Issue Date: Concurrently

Entitled: Circuit configuration and method of generating the drive signal of the deflection transistor of a cathode ray tube

Koninklijke Philips Electronics N.V., a corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

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2. ☐ an assignee of less than the entire right, title and interest.
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The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

3/22/2007
Date

Kevin Simons, Reg. No. 45,110
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Signature

Patent Attorney
Title

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: TOLKIEHN, Robert Docket No.: **DE02 0024 US**

PTO Application No.: Conf.: Art Unit:

Date Filed: Examiner:

Title: Circuit configuration and method of generating the drive signal of the deflection transistor of a cathode ray tube

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Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

TRANSMITTAL OF
INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97

Sir:

Enclosed in this transmittal is an "Information Disclosure Statement by Applicant" and a copy of each of the documents listed thereon. These documents are considered to be relevant in that they have been cited as an "X" or "Y" document in a foreign Patent Office search report on a foreign counterpart application, a copy of which report is also enclosed.

☒ I hereby certify that these documents were cited in said search report not more than three (3) months prior to the filing of this information disclosure statement.

This disclosure is not an admission that any of these documents is material to or even prior art with respect to the above-referenced application.

The Commissioner is hereby requested and authorized pursuant to 37 CFR §1.136(a)(3), to treat any concurrent or future reply in this application requiring a petition for extension of time for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. Please charge any additional fees which may now or in the future be required in this application, including extension of time fees, but excluding the issue fee unless explicitly requested to do so, and credit any overpayment, to Deposit Account No. 14-1270.

Date: 7/22/2004

Respectfully submitted,

By _____

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" on the date indicated below.

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(Name) Daniel L. Michalik

Document5 (rev. 3/03)

INFORMATION DISCLOSURE STATEMENT BY APPLICANT		
	Application Number	
	Filing Date	
	First Named Inventor	TOLKIEHN, Robert
	Art Unit	
	Examiner Name	
	Attorney Docket Number	DE02 0024 US

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number No.-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns Lines, Where Relevant Passages or Relevant Figures Appear
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		EP 0 449 130	10-02-1991	CHRISTOPHER, TODD J.		

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in capital letters), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]

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INTERNATIONAL SEARCH REPORT

PCT/IB 03/00183

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04N3/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 42 40 876 A (THOMSON CONSUMER ELECTRONICS) 17 June 1993 (1993-06-17)	1-4,8
A	column 3, line 49 -column 4, line 38; figure 3	10-12
X	US 4 591 910 A (LAI STEPHEN H ET AL) 27 May 1986 (1986-05-27)	1-4,8
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A	US 4 968 919 A (OLIVER KIRK D) 6 November 1990 (1990-11-06) column 3, line 44 -column 4, line 4; figure 3A	1,4,8, 10-12

☐ Further documents are listed in the continuation of box C. ☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
11 April 2003	22/04/2003

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